CLAIMS

1. A method for use in a pipelined processor including a plurality of stages, the method comprising:

storing a first updated data address value in a future file; and

generating a second data address value from said first updated data address value.

2. The method of claim 1, further comprising storing said second data address value in the future file.

3. The method of claim 1, further comprising storing a committed data address value in an architectural file.

4. The method of claim 3, further comprising:

cancelling an instruction in the pipeline; and

restoring the future file to a valid state by writing the committed data address value in the architectural file to the future file.

5. The method of claim 1, wherein generating the second updated data address value comprises calculating the second updated data address value with a data address generator in an address calculation stage of the pipeline.

6. The method of claim 1, further comprising providing the future file in a decode stage of the pipeline.

7. The method of claim 1, wherein storing the first updated data address value comprises storing at least one of an index value, a length value, a base value, and a modify value in the future file.

8. An article comprising a machine-readable medium which stores machine-executable instructions, the instructions causing a machine to:

store a first updated data address value in a future file; and

generate a second data address value from said first updated data address value.

9. The article of claim 8, further comprising instructions which cause the machine to store said second data address value in the future file.

10. The article of claim 8, further comprising instructions which cause the machine to store a committed data address value in an architectural file.

11. The article of claim 10, further comprising instructions which cause the machine to:

cancel an instruction in the pipeline; and

restore the future file to a valid state by writing the committed data address value in the architectural file to the future file.

12. The article of claim 8, wherein the instructions which cause the machine to generate the second updated data address value comprise instructions which cause the machine to calculate the second updated data address value with a data address generator in an address calculation stage of the pipeline.

13. The article of claim 8, further comprising instructions which cause the machine to provide the future file in a decode stage of the pipeline.

14. The article of claim 8, wherein the instructions which cause the machine to store the first updated data address value comprise instructions which cause the machine to store at least one of an index value, a length value, a base value, and a modify value in the future file.

15. A processor comprising:

a pipeline comprising two or more stages;

a future file operative to store a first updated data address value;

a data address generator operative to generate a second updated data address value from said first updated data address value; and

an update bus connected between the data address generator and the future file and operative to write the second updated data address value to the future file.

16. The processor of claim 15, wherein said two or more stages include a decode stage, an address calculation stage, an execution stage, and a write back stage.

17. The processor of claim 16, wherein the future file is located in the decode stage and the data address generator is located in the address calculation stage.

18. The processor of claim 15, further comprising an architectural file operative to store committed data addresses values.

19. The processor of claim 18, further comprising a restore bus connected between the architectural file and the future file; and

a control unit operative to write the committed data address values from the architectural file to the future file via the restore bus in response to the pipeline being cancelled.

20. The processor of claim 15, wherein the first updated data address value includes at least one of an index value, a length value, a base value, and a modify value.

21. The processor of claim 15, wherein the processor comprises a digital signal processor.

22. A system comprising:

a static random access memory; and

a processor coupled to the static random access memory and including

a pipeline comprising two or more stages,

a future file operative to store a first updated data address value,

a data address generator operative to generate a second updated data address value from said first updated data address value, and

an update bus connected between the data address generator and the future file and operative to write the second updated data address value to the future file.

23. The system of claim 22, wherein said two or more stages include a decode stage, an address calculation stage, an execution stage, and a write back stage.

24. The system of claim 23, wherein the future file is located in the decode stage and the data address generator is located in the address calculation stage.

25. The system of claim 22, further comprising an architectural file operative to store committed data addresses values.

26. The system of claim 25, further comprising a restore bus connected between the architectural file and the future file; and

a control unit operative to write the committed data address values from the architectural file to the

future file via the restore bus in response to the pending pipeline instructions being cancelled.

27. The system of claim 22, wherein the first updated data address value includes at least one of an index value, a length value, a base value, and a modify value.

28. The system of claim 22, wherein the processor comprises a digital signal processor.